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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/809,044 | 03/25/2004 | Shiro Fujima | NEKU 21.077 (100806-00256 | 5789 |

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KATTEN MUCHIN ROSENMAN LLP
575 MADISON AVENUE
NEW YORK, NY 10022-2585

| EXAMINER | |
|---|---|
| MAI, SON LUU | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2827 | |

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/809,044 | FUJIMA, SHIRO | |
| | Examiner | Art Unit | |
| | Son L. Mai | 2827 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,10-14,20 and 21* is/are rejected.

7)☒ Claim(s) *5-9 and 15-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06-09-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. The papers filed 07-22-05 have been entered. The objections to claims 1 and 11, and the rejection to claim 21 are withdrawn in view of the amendments to the claims. Accordingly, claims 1-21 are still pending.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 10-14, 20 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 6,163,488 issued to Tanizaki et al. (hereinafter being referred to as "Tanizaki").

Regarding claims 1 and 11, Tanizaki discloses a redundancy control circuit (figure 12) comprising: a plurality of program elements (anti-fuse 1), in which a defect address indicating a position of a defect is programmed by a dielectric breakdown due to applying of a voltage (signal BST and column 5, lines 11-21); and a voltage control section (which generates signal BST) which applies said voltage to part of a plurality of targeted program elements simultaneously, wherein said plurality of targeted program elements is part of said plurality of program element to be dielectrically broken down correspondingly to said defect address.

Regarding claims 2 and 12, Tanizaki discloses a number of said part of the plurality of targeted program elements, of which number is less than a number of said

plurality of program elements, is one (when one defective address is programmed), and said voltage control section applies said voltage to each of said plurality of targeted program elements, one by one.

Regarding claims 3 and 13, Tanizaki teaches that the voltage control section applies said voltage (BST) to said plurality of targeted program elements, at a timing of a trigger signal (RAS is active as shown in figure 13).

Regarding claims 4 and 14, Tanizaki shows that the voltage control section commonly applies said voltage (BST) to said plurality of targeted program elements (1), and said voltage is a voltage generated inside a device including said redundancy control circuit (column 9, lines 35-40).

Regarding claims 10 and 20, Tanizaki shows in figure 12, the program element (1) is an anti-fuse.

Regarding claim 21, Tanizaki teaches at last paragraph of column 3 that the program element is a capacitor in a DRAM.

***Allowable Subject Matter***

4. Claims 5-9 and 15-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach the further limitation of the voltage control section including: a timing setting section which outputs a timing signal indicating a

timing for carrying out a dielectric breakdown of each of the plurality of program elements based on a trigger signal.

***Response to Arguments***

6. Applicant's arguments filed 07-22-05 have been fully considered but they are not persuasive. In the Remarks, on page 10 and 11, the Applicant argued that the applied reference to Tanizaki only shows a single program element 1 in both figures 1 and 4 and Tanizaki does not show a plurality of program elements as claimed in claim 1. On the contrary, as pointing out in the previous Office action, Tanizaki illustrates in figure 12 the plurality of program elements 1 in fuse circuits 10 (Each fuse circuit 10 includes a program element 1). Additionally, the Applicant argued that Tanizaki does not disclose or suggest a voltage control section which applies a voltage to part of a plurality of targeted program elements simultaneously. On the contrary, at column 12, lines 4-10, Tanizaki states the antifuses of fuse circuit 10.1 to 10.n are blown with defective addresses. Thus, Tanizaki teaches all the limitations as claimed in the rejected claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

10-03-05

Son L. Mai
Primary Examiner
Art Unit 2827